CLAIMS

What is claimed is:

1. A content addressable memory (CAM) device comprising:

a first plurality of CAM cells each including a first static storage circuit to store a first data value;

a first pair of bit lines coupled to the first plurality of CAM cells; and

a first sense amplifier including a first transistor having first and second terminals coupled to first and second bit lines, respectively, of the first pair of bit lines.

2. The CAM device of claim 1 wherein the first sense amplifier further includes a second transistor having first and second terminals coupled to the first and second bit lines, respectively.

3. The CAM device of claim 2 wherein the first sense amplifier further includes a third transistor having a first terminal and wherein the first and second transistors have respective third terminals coupled to one another and to the first terminal of the third transistor.

4. The CAM device of claim 3 wherein the third transistor has a second terminal coupled to receive a control signal and a third terminal coupled to a reference voltage node, the third transistor being switched to a conducting state in response to the control signal to enable the first and second transistors to affect states of the first and second bit lines.

5. The CAM device of claim 1 wherein the first terminal of the first transistor is a control terminal, and the second terminal of the second transistor is a control terminal.

6. The CAM device of claim 5 wherein the second terminal of the first transistor is an output terminal, and the first terminal of the second transistor is an output terminal.

7. The CAM device of claim 1 wherein the first terminal of the first transistor is a gate terminal and the second terminal of the first transistor is a drain terminal.

8. The CAM device of claim 7 wherein the first sense amplifier further includes a second transistor having a gate terminal coupled to the second bit line and a drain terminal coupled to the first bit line.

9. The CAM device of claim 1 wherein the first static storage circuit comprises first and second inverters having respective input and output nodes, the output node of the first inverter being coupled to the input node of the second inverter and the output node of the second inverter being coupled to the input node of the first inverter.

10. The CAM device of claim 1 wherein the first pair of bit lines is coupled to the first static storage circuit within each of the first plurality of CAM cells.

11. The CAM device of claim 10 wherein the first static storage circuit comprises first and second access-enable transistors, the first access-enable transistor being coupled between the input node of the first inverter and a first bit line of the first pair of bit lines, and the second access-enable transistor being coupled between the input node of the second inverter and a second bit line of the first pair of bit lines.

12. The CAM device of claim 11 further comprising a first word line coupled to control

terminals of the first and second access-enable transistors.

13. The CAM device of claim 1 further comprising a pair of compare lines coupled to the first plurality of CAM cells, and wherein each of the first plurality of CAM cells includes a compare circuit coupled to the pair of compare lines and to the first static storage circuit.

14. The CAM device of claim 13 wherein each of the first plurality of CAM cells further includes a second static storage circuit coupled to the compare circuit of the CAM cell and configured to store a second data value.

15. The CAM device of claim 14 wherein the second data value is a mask value and wherein the compare circuit includes at least one mask transistor coupled to receive the mask value from the second static storage circuit.

16. The CAM device of claim 14 further comprising a plurality of match lines and wherein the compare circuit of each CAM cell includes first and second transistors coupled in series between a reference voltage node and a respective one of the plurality of match lines, and third and fourth transistors coupled in series between the reference voltage node and a respective one of the plurality of match lines, wherein a control terminal of the first transistor is coupled to the first static storage circuit and a control terminal of the third transistor is coupled to the second static storage circuit.

17. The CAM device of claim 14 wherein the second transistor is coupled to a first compare line of the pair of compare lines and the fourth transistor is coupled to a second compare line of the pair of compare lines.

18. The CAM device of claim 1 further comprising:

a second pair of bit lines;

a first transistor coupled between a first bit line of the first pair of bit lines and a first bit line of the second pair of bit lines; and

a second transistor coupled between a second bit line of the first pair of bit lines and a second bit line of the second pair of bit lines.

19. The CAM device of claim 18 further comprising:

a second plurality of CAM cells;

a third pair of bit lines coupled to the second plurality of CAM cells;

a third transistor coupled between a first bit line of the third pair of bit lines and the first bit line of the second pair of bit lines; and

a fourth transistor coupled between a second bit line of the third pair of bit lines and the second bit line of the second pair of bit lines.

20. The CAM device of claim 19 wherein the CAM device further comprises a second sense amplifier coupled to the third pair of bit lines.

21. The CAM device of claim 20 wherein the second sense amplifier comprises a first transistor having first and second terminals coupled to the first and second bit lines, respectively, of the third pair of bit lines.

22. The CAM device of claim 18 further comprising a second sense amplifier coupled to the second pair of bit lines.

23. The CAM device of claim 22 wherein the second sense amplifier comprises a first transistor having first and second terminals coupled to the first and second bit lines, respectively, of the second pair of bit lines.

24. The CAM device of claim 1 wherein the first sense amplifier further includes second and third transistors, the first terminal of the first transistor being coupled to the first bit line via the second transistor, and the second terminal of the first transistor being coupled to the second bit line via the third transistor.

25. The CAM device of claim 24 wherein the first sense amplifier further includes a fourth transistor having a first and second terminals, the first terminal of the fourth transistor being coupled to the second bit line via the third transistor, and the second terminal of the fourth transistor being coupled to the first bit line via the second transistor.

26. The CAM device of claim 25 wherein the first and fourth transistors have respective third terminals coupled to one another.

27. A content addressable memory (CAM) device comprising:

a plurality of CAM cell groups each including a respective plurality of CAM cells;

a plurality of pairs of group bit lines, each pair of group bit lines being coupled to the plurality of a CAM cells of a respective one of the CAM cell groups;

a plurality of group sense amplifiers coupled respectively to the plurality of pairs of group bit lines; and

at least one compare line coupled to the plurality of CAM cells in each of the plurality of CAM cell groups.

28. The CAM device of claim 27 further comprising a pair of column bit lines coupled to each pair of group bit lines by a respective pair of group-access transistors.

29. The CAM device of claim 28 further comprising a column sense amplifier coupled to the pair of column bit lines.

30. The CAM device of claim 28 wherein each of the plurality of CAM cells of a CAM cell group comprises:

a storage element;

a compare circuit coupled to the storage element; and

a pair of storage-access transistors coupled between the storage element and the pair of group bit lines coupled to the plurality of CAM cells of the CAM cell group.

31. The CAM device of claim 30 further comprising a plurality of row word lines coupled to control terminals of the storage-access transistors, and a plurality of group word lines coupled to control terminals of the group-access transistors.

32. The CAM device of claim 31 further comprising:

a first decoder circuit to activate one of the plurality of row word lines indicated by a first portion of an address value; and

a second decoder circuit to activate one of the plurality of group word lines indicated by a second portion of the address value.

33. The CAM device of claim 32 further comprising a control circuit to output a first decode-enable signal to the first decoder circuit and to output a second decode-enable signal to the

second decoder circuit, the first decoder circuit being configured to activate the one of the plurality of row word lines in response to the first decode-enable signal, and the second decoder circuit being configured to activate the one of the group word lines in response to the second decode-enable signal.

34. The CAM device of claim 33 wherein the control circuit is configured to output the first decode-enable signal and second decode-enable signals at different times.

35. A method of operation within a content addressable memory (CAM) device, the method comprising:

switchably forming a path between a static storage circuit of a CAM cell and a first bit line to reduce a voltage of the first bit line to a first level; and

sinking current within a first sense amplifier coupled to the first bit line to reduce the voltage of the first bit line to a second level that is lower than the first level.

36. The method of claim 35 wherein switchably forming a path between a static storage circuit and a first bit line comprises activating a word line coupled to a control terminal of a first transistor, the first transistor being coupled between the first bit line and the static storage circuit.

37. The method of claim 35 wherein switchably forming a path between a static storage circuit and a first bit line comprises switchably forming a path between a first output node of the static storage element and the first bit line, the method further comprising switchably forming a path between a second output node of the static storage element and a second bit line, the second output node having a higher voltage level than the first output node such

that the voltage of the first bit line is reduced to a lower level than the voltage of the second bit line.

38. The method of claim 35 further comprising outputting an enable signal to the first sense amplifier to enable the first sense amplifier to sink current.

39. The method of claim 35 wherein the first sense amplifier comprises a first transistor having a drain terminal coupled to the first bit line, a source terminal coupled to a first node, and a gate terminal coupled to a second bit line, the first transistor drawing current from the first bit line when a voltage on the second bit line is higher than the first level.

40. The method of claim 39 wherein the first sense amplifier further comprises a second transistor having a drain terminal coupled to the first node, a source terminal coupled to a reference voltage node and a gate terminal coupled to receive an enable signal, the second transistor forming a path between the first node and the reference voltage node in response to the enable signal.

41. The method of claim 35 further comprising switchably forming a path between the first bit line and a second bit line to reduce a voltage of the second bit line to a third level.

42. The method of claim 41 further comprising sinking current within a second sense amplifier coupled to the second bit line to reduce the voltage of the second bit line to a fourth level that is lower than the third level.

43. A method of operation within a content addressable memory (CAM) device, the method comprising:

enabling a write driver to draw current from a first bit line to reduce a voltage of the first bit line from a precharged level to a first reduced level;

enabling a sense amplifier to draw current from the first bit line to reduce the voltage of the first bit line from the first reduced level to a second reduced level; and

switchably forming a path between the first bit line and a static storage circuit of a CAM cell to enable the second reduced level of the first bit line to switch the static storage circuit from a first state to a second state.

44. The method of claim 43 wherein enabling the sense amplifier to draw current from the first bit line comprises enabling the sense amplifier to draw current from the first bit line after enabling the write driver to draw current from the first bit line.

45. The method of claim 43 wherein enabling the write driver to draw current from the first bit line comprises outputting a write enable signal to the write driver, and wherein enabling the sense amplifier to draw current from the first bit line comprises outputting a sense enable signal to the sense amplifier.

46. The method of claim 45 wherein switchably forming a path between the first bit line and a static storage circuit of a CAM cell comprises switchably forming the path between the first bit line and the static storage circuit after outputting the write enable signal and the sense enable signal.

47. The method of claim 43 wherein enabling the sense amplifier to draw current from the first bit line comprises enabling the sense amplifier to draw current from the first bit line after enabling the write driver to draw current from the first bit line, the combined current drawn

by the write driver and sense amplifier acting to reduce the first bit line to the second reduced level.

48. A content addressable memory (CAM) device comprising:

a CAM cell having static storage means for static storage of a data value;

a first bit line;

means for switchably forming a path between the static storage means and the first bit line to reduce a voltage of the first bit line to a first level; and

a first sense amplifier coupled to the first bit line and having means for drawing current from the first bit line to reduce the voltage of the first bit line to a second level that is lower than the first level.

49. The CAM device of claim 48 further comprising:

a second bit line; and

means for switchably forming a path between the first bit line and a second bit line to reduce a voltage of the second bit line to a third level.

50. The CAM device of claim 49 further comprising a second sense amplifier having means for drawing current from the second bit line to reduce the voltage of the second bit line to a fourth level that is lower than the third level.

51. A content addressable memory (CAM) device comprising:

a CAM cell having static storage means for static storage of a data value;

a first bit line;

write driver means for drawing current from the first bit line during a first interval to

reduce a voltage of the first bit line to a first reduced level;

sense amplifier means for drawing current from the first bit line during a second interval to reduce the voltage of the first bit line to a second reduced level, the second interval beginning after the first interval and being at least partially encompassed by the first interval; and

means for forming a path between the first bit line and the static storage means.